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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/915,833	07/26/2001	Kalvin E. Williams	01-213 1496.00136	7179

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EXAMINER	
COURTENAY III, ST JOHN	
ART UNIT	**PAPER NUMBER**
2126	2

DATE MAILED: 05/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/915,833	Applicant(s) WILLIAMS ET AL.	
	Examiner St. John Courtenay III	Art Unit 2126	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

ST. JOHN COURTENAY III
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1- 20 are rejected under 35 U.S.C. § 102(b) as being anticipated by **Yamada et al.** (U.S. Patent 5,617,537).

As per independent claim 1:
Yamada teaches an apparatus comprising:

- a shared memory configured to store data [see col. 3, line 55, "distributed shared memories" col. 7, line 46]; and
- a multiprocessor logic circuit comprising a plurality of processors and a message circuit, wherein the message circuit is configured to pass messages between the processors [see "processor interconnect 25" and associated discussion col. 7, lines 10-15].

As per independent claim 12:
This claim is rejected for the same reasons detailed above in the rejection of independent claim 1, and also for the following additional reasons:

Yamada teaches an apparatus comprising:

- means for storing data with a shared memory [see col. 3, line 55, "distributed shared memories" col. 7, line 46];
- means for processing data a with a plurality of processors [see multiprocessor system 17, col. 7, line 12]; and
- means for passing messages between the processors [see transferring messages between the processors discussion col. 7, lines 10-22].

As per independent claim 13:
This claim is rejected for the same reasons detailed above in the rejection of the preceding independent claims, and also for the following additional reasons:

Yamada teaches a method for multiprocessor communication with a shared memory, comprising the steps of:

(A) storing data with the shared memory [see col. 3, line 55, "distributed shared memories" col. 7, line 46];

(B) processing data with a plurality of processors [see multiprocessor system 17, col. 7, line 12]; and

(C) passing messages between the processors [see transferring messages between the processors discussion col. 7, lines 10-22].

As per dependent claim 2:
Yamada teaches the message circuit comprises a dedicated messaging circuit [see message buffer discussion, col. 8, beginning line 4].

As per dependent claim 3:
Yamada teaches the message circuit comprises a message pipe-line FIFO [see FIFO col. 7, line 50; see FIFO col. 8, line 45, line 55; col. 10, lines 14, 18 & 21; see also ENQ and DEQ operations associated with a FIFO data structure, col. 23, lines 25-61].

As per dependent claim 4:
Yamada teaches the message circuit is further configured to provide bi-directional orderly command passing [see "bi-directional communication" and associated discussion col. 46, beginning line 9].

As per dependent claim 5:
Yamada teaches the message circuit is further configured to generate one or more control signals, the control signals configured to control an operation of the processors [see message buffer discussion, col. 8, beginning line 4; see "distributed shared memory control means" and associated discussion col. 4, line 43].

As per dependent claim 6:
Yamada inherently teaches the control signals comprise signals selected from the group consisting of (i) pipeline overflow signals, (ii) pipeline available signals, and (iii) command pending signals [see the rejection of claim 3 above for FIFO (pipeline) references].

As per dependent claim 7:
Yamada teaches the message circuit is further configured to add commands with normal priority levels and urgent priority levels

[see FIFO col. 7, line 50; see FIFO col. 8, line 45, line 55; col. 10, lines 14, 18 & 21; see also ENQ and DEQ operations associated with a FIFO data structure, col. 23, lines 25-61 – i.e., the head of a FIFO queue has a higher priority than the rear of the FIFO queue].

As per dependent claim 8:
Yamada teaches the normal priority levels comprise adding commands to an end of a message queue and the urgent priority levels comprise adding commands to a near to front of the message queue [see FIFO col. 7, line 50; see FIFO col. 8, line 45, line 55; col. 10, lines 14, 18 & 21; see also ENQ and DEQ operations associated with a FIFO data structure, col. 23, lines 25-61– i.e., the head of a FIFO queue has a higher priority than the rear of the FIFO queue].

As per dependent claim 9:
Yamada inherently teaches the multiprocessor logic circuit further comprises an address decoder configured to decode a system address and control the message circuit [see addressing discussion col. 14, lines 45-56].

As per dependent claim 10:
Yamada teaches the apparatus provides a multiprocessor communication and shared memory architecture [see multiprocessor and shared memory discussion col. 4, lines 31-58].

As per dependent claim 11:
Yamada teaches:

- the multiprocessor logic circuit and the shared memory are coupled by a system bus [see "system bus" and associated discussion col. 7, line 13];

- the multiprocessor logic block further comprises an address decoder configured to control the message circuit [see addressing discussion col. 14, lines 45-56]; and

- the message circuit is configured to generate one or more control signals configured to control the processors [see "control signals" and associated discussion, col. 12, line 51] .

As per dependent claim 14:
Yamada teaches wherein step (C) further comprises: providing bi-directional orderly command passing [see the rejection of claim 4 above].

As per dependent claim 15:
Yamada teaches step (C) further comprises: generating one or more control signals, the control signals configured to control an operation of the processors [see the rejection of claim 5 above].

As per dependent claim 16:
Yamada teaches the control signals comprise signals selected from the group consisting of: (i) pipe-line overflow signals, (ii) pipe-line available signals, and (iii) command pending signals [see the rejection of claim 6 above].

As per dependent claim 17:
Yamada teaches wherein step (C) further comprises: adding commands with normal priority levels; and adding commands with urgent priority levels [see the rejection of claim 7 above].

As per dependent claim 18:
Yamada teaches the adding commands with normal priority levels further comprises adding commands to an end of a message queue; and the adding commands with urgent priority

levels further comprises adding commands to a near to front of the message queue [see the rejection of claim 8 above].

As per dependent claim 19:
Yamada teaches wherein step (C)
further comprises decoding a system address [see the rejection of claim 9 above].

As per dependent claim 20:
Yamada teaches wherein step (C) further comprises: controlling the messages in response to the decoded system address [see addressing discussion col. 14, lines 45-56].

Prior Art not relied upon:
Please refer to the references listed on the attached PTO-892 which are not relied upon in the claim rejections detailed above.

How to Contact the Examiner:

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **St. John Courtenay III** whose voice telephone number is **(703) 308-5217.** A voice mail service is also available at this number. Normal Flex work schedule: M – F 7:30 AM - 4:00 PM

- **All responses sent by U.S. Mail should be mailed to:**

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

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http://www.uspto.gov/web/offices/pac/dapp/opla/preognotice/faxnotice.pdf

Effective Oct. 15, 2003, ALL patent application correspondence transmitted by FAX must be directed to the new PTO central FAX number:

NEW PTO CENTRAL FAX NUMBER:
703-872-9306

- Any inquiry of a general nature or relating to the status of this application should be directed to the **TC 2100 Group receptionist: (703) 305-3900.**

Please direct inquiries regarding fees, paper matching, and other issues not involving the Examiner to:
Technical Center 2100 CUSTOMER SERVICE: 703 306-5631

The Manual of Patent Examining Procedure (MPEP) is available online at:
http://www.uspto.gov/web/offices/pac/mpep/index.html

ST. JOHN COURTENAY III
PRIMARY EXAMINER